CS5421

Dual Out-of-Phase Synchronous Buck Controller with Remote Sense

The CS5421 is a dual N−channel synchronous buck regulator controller. It contains all the circuitry required for two independent buck regulators and utilizes the V^2™ control method to achieve the fastest possible transient response and best overall regulation, while using the least number of external components. The CS5421 features out−of−phase synchronization between the channels, reducing the input filter requirement. The CS5421 also provides undervoltage lockout, Soft Start, built in adaptive FET non−overlap and remote sense capability. The part is available in a 16 Lead SO Narrow package allowing the designer to minimize solution size.

Features

- V^2 Control Topology
- 150 ns Transient Response
- Programmable Soft Start
- 25 ns Gate Rise and Fall Times (with 1.0 nF load)
- 40 ns Adaptive FET Nonoverlap Time
- 100% Duty Cycle for Enhanced Transient Response
- Internal Slope Compensation
- 1.0 V 0.8% and 2.0% Error Amplifier References
- 150 kHz to 750 kHz Programmable Frequency Operation
- Switching Frequency Set by Single Resistor
- Out−Of−Phase Synchronization Between the Channels Reduces the Input Filter Requirement
- Undervoltage Lockout
- On/Off Control Through Use of the COMP Pins

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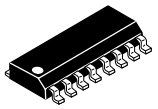
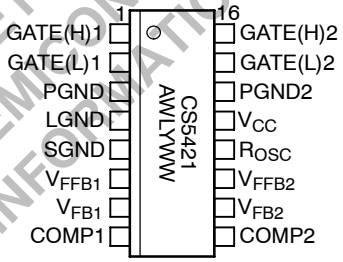


SO−16
D SUFFIX
CASE 751B

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS5421GD16	SO−16	48 Units/Rail
CS5421GDR16	SO−16	2500 Tape & Reel

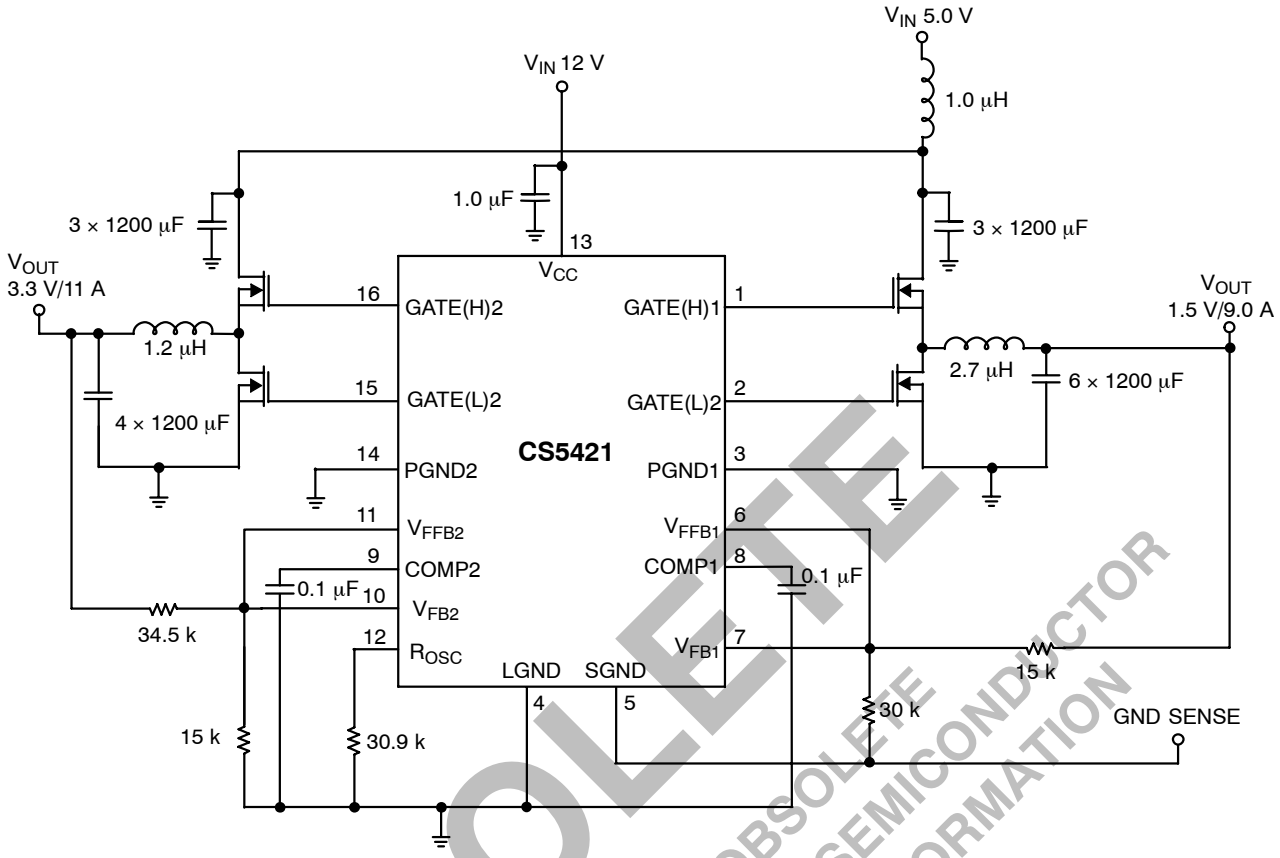


Figure 1. Application Diagram, 5.0 V/12 V to 3.3 V/11 A and 1.5 V/9.0 A Converter for Processor I/O and Core Supplies

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T_J	150	°C
Storage Temperature Range, T_S	−65 to +150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Package Thermal Resistance: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 28 115	 °C/W °C/W
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_{CC}	IC Power Input	16 V	−0.3 V	N/A	1.5 A peak 200 mA DC
COMP1, COMP2	Compensation Capacitor for Channel 1 or 2	4.0 V	−0.3 V	1.0 mA	1.0 mA
V_{FB1}, V_{FB2}	Voltage Feedback Input for Channel 1 or 2	5.0 V	−0.3 V	1.0 mA	1.0 mA
V_{FB1}, V_{FB2}	Fast Voltage Feedback Input for Channel 1 or 2	5.0 V	−0.3 V	1.0 mA	1.0 mA

ABSOLUTE MAXIMUM RATINGS (continued)

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
R_{OSC}	Oscillator Resistor	4.0 V	−0.3 V	1.0 mA	1.0 mA
GATE(H)1, GATE(H)2	High−Side FET Driver for Channel 1 or 2	16 V	−0.3 V	1.5 A peak 200 mA DC	1.5 A peak 200 mA DC
GATE(L)1, GATE(L)2	Low−Side FET Driver for Channel 1 or 2	16 V	−0.3 V	1.5 A peak 200 mA DC	1.5 A peak 200 mA DC
PGND1	Power Ground for Channel 1	0 V	0 V	1.5 A peak 200 mA DC	N/A
PGND2	Power Ground for Channel 2	0 V	0 V	1.5 A peak 200 mA DC	N/A
SGND	Ground for Internal Reference	150 mV	0 V	1.0 mA	N/A
LGND	Logic Ground	0 V	0 V	50 mA	N/A

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; R_{OSC} = 30.9 k, $C_{COMP1,2}$ = 0.1 μF, 10.8 V < V_{CC} < 13.2 V; $C_{GATE(H)1,2} = C_{GATE(L)1,2}$ = 1.0 nF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
$V_{FB1(2)}$ Bias Current	$V_{FB1(2)}$ = 0 V	–	0.1	1.0	μA
COMP1,2 Source Current	COMP1,2 = 1.2 V to 2.5 V; $V_{FB1(2)}$ = 0.8 V	15	30	60	μA
COMP1,2 Sink Current	COMP1,2 = 1.2 V; $V_{FB1(2)}$ = 1.2 V	15	30	60	μA
Reference Voltage 1	COMP1 = V_{FB1}; $25°C < T_J < 125°C$	0.992	1.000	1.008	V
Reference Voltage 2	COMP2 = V_{FB2}	0.980	1.000	1.020	V
COMP1,2 Max Voltage	$V_{FB1(2)}$ = 0.8 V	3.0	3.3	–	V
COMP1,2 Min Voltage	$V_{FB1(2)}$ = 1.2 V	–	0.25	0.35	V
Open Loop Gain	–	–	95	–	dB
Unity Gain Band Width	–	–	40	–	kHz
PSRR @ 1.0 kHz	–	–	70	–	dB
Transconductance	–	–	32	–	mmho
Output Impedance	–	–	2.5	–	MΩ
GATE(H) and GATE(L)					
High Voltage (AC)	Measure: V_{CC} − GATE(L)1,2; V_{CC} − GATE(H)1,2; Note 2	–	0	0.5	V
Low Voltage (AC)	Measure:GATE(L)1,2 or GATE(H)1,2; Note 2	–	0	0.5	V
Rise Time	1.5 V < GATE(L)1,2 < V_{CC} − 1.5 V 1.5 V < GATE(H)1,2 < V_{CC} − 1.5 V	–	25	60	ns
Fall Time	V_{CC} − 1.5 > GATE(L)1,2 > 1.5 V V_{CC} − 1.5 > GATE(H)1,2 > 1.5 V	–	20	60	ns
GATE(H) to GATE(L) Delay	GATE(H)1,2 < 1.0 V, GATE(L)1,2 > 1.0 V	40	70	100	ns
GATE(L) to GATE(H) Delay	GATE(L)1,2 < 1.0 V, GATE(H)1,2 > 1.0 V	40	70	100	ns
GATE(H)1(2) and GATE(L)1(2) pull−down	Resistance to PGND Note 2	50	125	280	kΩ

2. Guaranteed by design, not 100% tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; R_{OSC} = 30.9 k, $C_{COMP1,2}$ = 0.1 μF, 10.8 V < V_{CC} < 13.2 V; $C_{GATE(H)1,2} = C_{GATE(L)1,2}$ = 1.0 nF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
PWM Comparator					
Transient Response	COMP1,2 = 1.0 V, $V_{FB1(2)} = V_{FFB1(2)}$ = 0 to 1.2 V	–	150	300	ns
PWM Comparator Offset	$V_{FFB1(2)}$ = 0 V; Increase COMP1,2 until GATE(H)1,2 starts switching	0.30	0.45	0.60	V
Artificial Ramp	Duty cycle = 50%, Note 3	40	70	100	mV
$V_{FFB1(2)}$ Bias Current	$V_{FFB1(2)}$ = 0 V	–	0.4	1.5	μA
$V_{FFB1(2)}$ Input Range	–	0.0	–	1.1	V
Minimum Pulse Width	–	–	–	300	ns
Oscillator					
Switching Frequency	R_{OSC} = 61.9 k; Measure GATE(H)2, Note 3	112	150	188	kHz
Switching Frequency	R_{OSC} = 30.9 k; Measure GATE(H)2	224	300	376	kHz
Switching Frequency	R_{OSC} = 11.8 k; Measure GATE(H)2, Note 3	600	750	900	kHz
R_{OSC} Voltage	R_{OSC} = 30.9 k, Note 3	0.970	1.000	1.030	V
Phase Difference	–	–	180	–	°
Supply Currents					
V_{CC} Current	COMP1,2 = 0 V (No Switching)	–	16	22	mA
SGND Current	–	75	150	225	μA
Undervoltage Lockout					
Start Threshold	GATE(H) Switching; COMP1,2 charging	7.8	8.6	9.6	V
Stop Threshold	GATE(H) not switching; COMP1,2 discharging	7.0	7.8	8.6	V
Hysteresis	Start−Stop	0.5	0.8	1.5	V

3. Guaranteed by design, not 100% tested in production.

PACKAGE PIN DESCRIPTION

PACKAGE PIN # 16 Lead SO Narrow	PIN SYMBOL	FUNCTION
1	GATE(H)1	High Side Switch FET driver pin for the channel 1 FET.
2	GATE(L)1	Low Side Synchronous FET driver pin for the channel 1 FET.
3	PGND1	High Current ground for the GATE(H)1 and GATE(L)1 pins.
4	LGND	Logic ground. All control circuits are referenced to this pin. IC substrate connection.
5	SGND	Ground sense for the internal reference.
6	V_{FFB1}	Input for the channel 1 PWM comparator.
7	V_{FB1}	Error amplifier inverting input for channel 1.
8	COMP1	Channel 1 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation. The same capacitor provides Soft Start timing for channel 1. This pin also disables the channel 1 output when pulled below 0.3 V.
9	COMP2	Channel 2 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation and Soft Start timing for channel 2. Channel 2 output is disabled when this pin is pulled below 0.3 V.

PACKAGE PIN DESCRIPTION (continued)

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16 Lead SO Narrow		
10	V_{FB2}	Error amplifier inverting input for channel 2.
11	V_{FFB2}	Input for the channel 2 PWM comparator.
12	R_{OSC}	A resistor from this pin to ground sets switching frequency.
13	V_{CC}	Input Power supply pin.
14	PGND2	High Current ground for the GATE(H)2 and GATE(L)2 pins.
15	GATE(L)2	Low Side Synchronous FET driver pin for the channel 2 FET.
16	GATE(H)2	High Side Switch FET driver pin for the channel 2 FET.

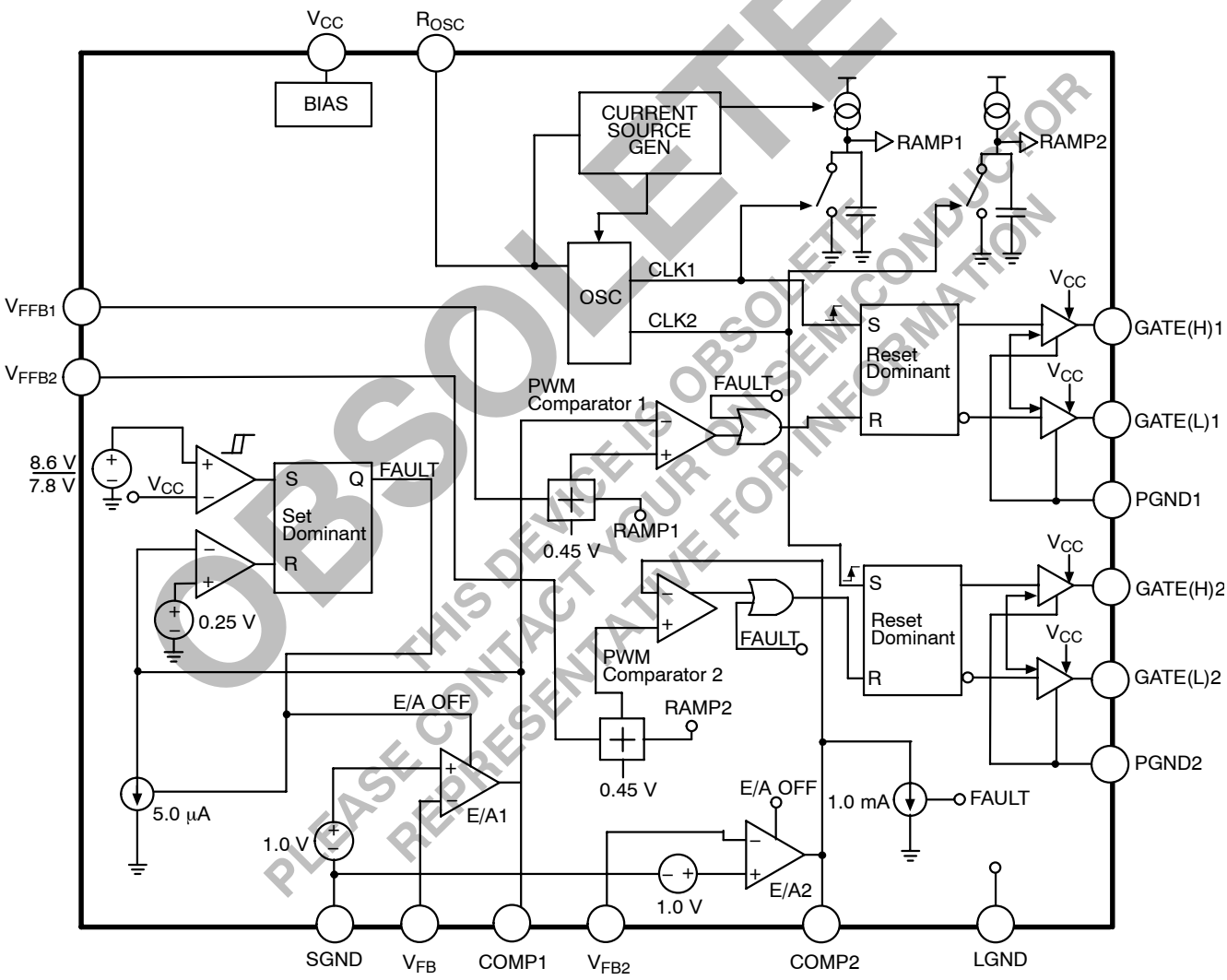


Figure 2. Block Diagram

APPLICATIONS INFORMATION

THEORY OF OPERATION

The CS5421 is a dual power supply controller that utilizes the V^2 control method. Two synchronous V^2 buck regulators can be built using a single controller. The fixed−frequency architecture, driven from a common oscillator, ensures a 180° phase differential between channels.

V^2 Control Method

The V^2 method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The V^2 method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

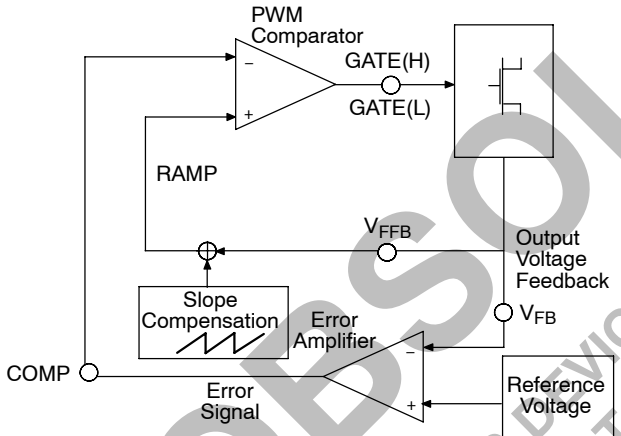


Figure 3. V^2 Control with Slope Compensation

The V^2 control method is illustrated in Figure 3. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the V^2 control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction time to the output load step is not related to the crossover frequency of the error signal loop.

The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this ‘slow’ feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation is drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulations. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity particularly at higher duty cycle (above 50%).

Startup

The CS5421 features a programmable Soft Start function, which is implemented through the Error Amplifier and the external Compensation Capacitor. This feature prevents stress to the power components and overshoot of the output voltage during start−up. As power is applied to the regulator, the CS5421 Undervoltage Lockout circuit (UVL) monitors the IC’s supply voltage (V_{CC}). The UVL circuit prevents the MOSFET gates from switching until V_{CC} exceeds the 8.6 V threshold. A hysteresis function of 800 mV improves noise immunity. The Compensation Capacitor connected to the COMP pin is charged by a 30 μA current source. When the capacitor voltage exceeds the 0.4 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is activated turning on the upper MOSFET. The current then ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the 0.4 V PWM comparator offset

threshold and the artificial ramp, the PWM comparator terminates the initial pulse.

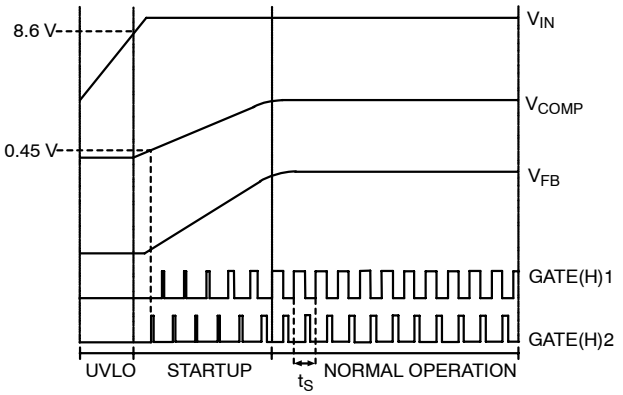


Figure 4. Idealized Waveforms

Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the V^2 control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading, according to the following graphs.

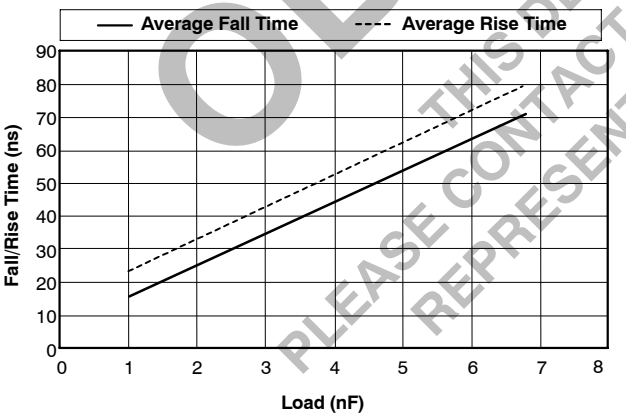


Figure 5. Average Rise and Fall Times

Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse−by−pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

Out−of−Phase Synchronization

In out−of−phase synchronization, the turn−on of the second channel is delayed by half the switching cycle. This delay is supervised by the oscillator, which supplies a clock signal to the second channel which is 180° out of phase with the clock signal of the first channel.

The advantages of out−of−phase synchronization are many. Since the input current pulses are interleaved with one another, the overlap time is reduced. The effect of this overlap reduction is to reduce the input filter requirement, allowing the use of smaller components. In addition, since peak current occurs during a shorter time period, emitted EMI is also reduced, thereby reducing shielding requirements.

Overvoltage Protection

Overvoltage Protection (OVP) is provided as a result of the normal operation of the V^2 control method and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

Remote Sense

When the load is far away from the regulator, the long feedback traces can cause additional voltage drop and induce noise which affects the accuracy of voltage regulation. A separate signal ground is provided to improve the noise immunity of remote voltage sensing. The 1.0 V reference voltage of the error amplifiers is directly referenced to this ground and no large currents flow through this ground during normal operation. The noise immunity and regulation accuracy can be improved significantly.

Output Enable

On/Off control of the regulator outputs can be implemented by pulling the COMP pins low. The COMP pins must be driven below the 0.4 V PWM comparator offset voltage in order to disable the switching of the GATE drivers.

DESIGN GUIDELINES

Definition of the design specifications

The output voltage tolerance can be affected by any or all of the following reasons:

1. buck regulator output voltage setpoint accuracy;
2. output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;

3. output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4. output voltage ripple and noise.

Budgeting the tolerance is left up to the designer who must take into account all of the above effects and provide an output voltage that will meet the specified tolerance at the load.

The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature.

Selecting Feedback Divider Resistors

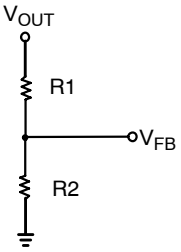


Figure 6. Selecting Feedback Divider Resistors

The feedback pins ($V_{FB1(2)}$) are connected to externalresistor dividers to set the output voltages. The error amplifier is referenced to 1.0 V and the output voltage is determined by selecting resistor divider values. Resistor R1 is selected based on a design trade−off between efficiency and output voltage accuracy. The output voltage error can be estimated due to the bias current of the error amplifier neglecting resistor tolerance:

$$\text{Error\%} = \frac{1 \times 10^{-6} \times R1}{1.0} \times 100\%$$

R2 can be sized after R1 has been determined:

$$R2 = R1\left(\frac{V_{OUT}}{1.0} - 1.0\right)$$

Calculating Duty Cycle

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$\text{Duty Cycle} = D = \frac{V_{OUT} + (V_{HFET} + V_L)}{V_{IN} + V_{LFET} - V_{HFET} - V_L}$$

where:

V_{OUT} = buck regulator output voltage;
V_{HFET} = high side FET voltage drop due to $R_{DS(ON)}$;
V_L = output inductor voltage drop due to inductor wire DC resistance;
V_{IN} = buck regulator input voltage;
V_{LFET} = low side FET voltage drop due to $R_{DS(ON)}$.

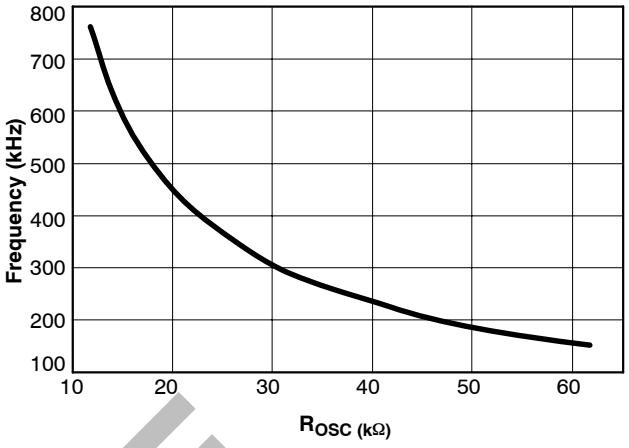


Figure 7. Switching Frequency

Selecting the Switching Frequency

Selecting the switching frequency is a trade−off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

The value of the oscillator resistor is designed to be linearly related to the switching period. If the designer prefers not to use Figure 7 to select the necessary resistor, the following equation quite accurately predicts the proper resistance for room temperature conditions.

$$R_{OSC} = \frac{21700 - f_{SW}}{2.31 f_{SW}}$$

where:

R_{OSC} = oscillator resistor in kΩ;
f_{SW} = switching frequency in kHz.

Selection of the Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss.

There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very commonly used. Powdered iron cores are very suitable due

to its high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The minimum value of inductance which prevents inductor saturation or exceeding the rated FET current can be calculated as follows:

$$L_{MIN} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{f_{SW} \times V_{IN(MIN)} \times I_{SW(MAX)}}$$

where:

L_{MIN} = minimum inductance value;
$V_{IN(MIN)}$ = minimum design input voltage;
V_{OUT} = output voltage;
f_{SW} = switching frequency;
$I_{SW(MAX)}$ − maximum design switch current.

The inductor ripple current can then be determined:

$$\Delta I_L = \frac{V_{OUT} \times (1.0 - D)}{L \times f_{SW}}$$

where:

ΔI_L = inductor ripple current;
V_{OUT} = output voltage;
L = inductor value;
D = duty cycle.
f_{SW} = switching frequency

The designer can now verify if the number of output capacitors will provide an acceptable output voltage ripple (1.0% of output voltage is common). The formula below is used:

$$\Delta I_L = \frac{\Delta V_{OUT}}{ESR_{MAX}}$$

Rearranging we have:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_L}$$

where:

ESR_{MAX} = maximum allowable ESR;
ΔV_{OUT} = 1.0% × V_{OUT} = maximum allowable output voltage ripple (budgeted by the designer);
ΔI_L = inductor ripple current;
V_{OUT} = output voltage.

The number of output capacitors is determined by:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$I_{L(PEAK)} = I_{OUT} + \frac{\Delta I_L}{2.0}$$

where:

$I_{L(PEAK)}$ = inductor peak current;
I_{OUT} = load current;
ΔI_L = inductor ripple current.

$$I_{L(VALLEY)} = I_{OUT} - \frac{\Delta I_L}{2.0}$$

where:

$I_{L(VALLEY)}$ = inductor valley current.

Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}}\right)$$

where:

$\Delta I_{OUT} / \Delta t$ = load current slew rate;
ΔI_{OUT} = load transient;
Δt = load transient duration time;
ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;
ESR = Maximum allowable ESR including capacitors and circuit traces;
t_{TR} = output voltage transient response time.

The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

ΔV_{ESR} = change in output voltage due to ESR (assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).
ESR = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$L_{IN} = \frac{\Delta V}{(dI/dt)_{MAX}}$$

where:

L_{IN} = input inductor value;

ΔV = voltage seen by the input inductor during a full load swing;

$(dI/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double−pole network with a slope of −2, a roll−off rate of −40 dB/dec, and a corner frequency:

$$f_C = \frac{1.0}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

SELECTION OF THE POWER FET

FET Basics

The use of the MOSFET as a power switch is propelled by two reasons: 1) *Its very high input impedance*; and 2) *Its very fast switching times*. The electrical characteristics of a MOSFET are considered to be those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of V_{GS}, and the faster the turn−on time. Power dissipation in the switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3) turn−on switching losses, 4) turn−off switching losses, and 5) gate−transitions losses. The latter three losses are proportional to frequency.

The most important aspect of FET performance is the Static Drain−To−Source On−Resistance ($R_{DS(ON)}$), which effects regulator efficiency and FET thermal management requirements. The On−Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On−Resistance also increases. Its positive temperature coefficient is between +0.6%/°C and +0.85%/°C. The higher the On−Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.

Both logic level and standard FETs can be used.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail−to−rail due to overshoot caused by the capacitive load they present to the controller IC.

Selection of the Switching (Upper) FET

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed 150°C.

The maximum RMS current through the switch can be determined by the following formula:

$$I_{RMS(H)} = \sqrt{\frac{\left[I_{L(PEAK)}^2 + (I_{L(PEAK)} \times I_{L(VALLEY)}) + I_{L(VALLEY)}^2 \times D\right]}{3.0}}$$

where:

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;

$I_{L(PEAK)}$ = inductor peak current;

$I_{L(VALLEY)}$ = inductor valley current;

D = duty cycle.

Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$P_{RMS(H)} = I_{RMS(H)}^2 \times R_{DS(ON)}$$

where:

$P_{RMS(H)}$ = switching MOSFET conduction losses;

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;

$R_{DS(ON)}$ = FET drain−to−source on−resistance

The upper MOSFET switching losses are caused during MOSFET switch−on and switch−off and can be determined by using the following formula:

$$P_{SWH} = P_{SWH(ON)} + P_{SWH(OFF)} = \frac{V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL})}{6.0T}$$

where:

$P_{SWH(ON)}$ = upper MOSFET switch−on losses;

$P_{SWH(OFF)}$ = upper MOSFET switch−off losses;
V_{IN} = input voltage;
I_{OUT} = load current;
t_{RISE} = MOSFET rise time (from FET manufacturer's switching characteristics performance curve);
t_{FALL} = MOSFET fall time (from FET manufacturer's switching characteristics performance curve);
$T = 1/f_{SW}$ = period.

The total power dissipation in the switching MOSFET can then be calculated as:

$$P_{HFET(TOTAL)} = P_{RMS(H)} + P_{SWH(ON)} + P_{SWH(OFF)}$$

where:
$P_{HFET(TOTAL)}$ = total switching (upper) MOSFET losses;
$P_{RMS(H)}$ = upper MOSFET switch conduction Losses;
$P_{SWH(ON)}$ = upper MOSFET switch−on losses;
$P_{SWH(OFF)}$ = upper MOSFET switch−off losses;

Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{HFET(TOTAL)} \times R_{\Theta JA}]$$

where:
T_J = FET junction temperature;
T_A = ambient temperature;
$P_{HFET(TOTAL)}$ = total switching (upper) FET losses;
$R_{\Theta JA}$ = upper FET junction−to−ambient thermal resistance.

Selection of the Synchronous (Lower) FET

The switch conduction losses for the lower FET can be calculated as follows:

$$P_{RMS(L)} = I_{RMS}^2 \times R_{DS(ON)}$$

$$= [I_{OUT} \times \sqrt{(1.0 - D)}]^2 \times R_{DS(ON)}$$

where:
$P_{RMS(L)}$ = lower MOSFET conduction losses;
I_{OUT} = load current;
D = Duty Cycle;
$R_{DS(ON)}$ = lower FET drain−to−source on−resistance.

The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non−overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$P_{SWL} = V_{SD} \times I_{LOAD} \times \text{non−overlap time} \times f_{SW}$$

where:
P_{SWL} = lower FET switching losses;
V_{SD} = lower FET source−to−drain voltage;
I_{LOAD} = load current;
Non−overlap time = GATE(L)−to−GATE(H) or GATE(H)−to−GATE(L) delay (from CS5421 data sheet Electrical Characteristics section);
f_{SW} = switching frequency.

The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$P_{LFET(TOTAL)} = P_{RMS(L)} + P_{SWL}$$

where:
$P_{LFET(TOTAL)}$ = Synchronous (lower) FET total losses;
$P_{RMS(L)}$ = Switch Conduction Losses;
P_{SWL} = Switching losses.

Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{LFET(TOTAL)} \times R_{\Theta JA}]$$

where:
T_J = MOSFET junction temperature;
T_A = ambient temperature;
$P_{LFET(TOTAL)}$ = total synchronous (lower) FET losses;
$R_{\Theta JA}$ = lower FET junction−to−ambient thermal resistance.

Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, V_{CC}, and the CS5421 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.

The IC power dissipation is determined by the formula:

$$P_{CONTROL(IC)} = I_{CC1}V_{CC1} + P_{GATE(H)1} + P_{GATE(L)1} + P_{GATE(H)2} + P_{GATE(L)2}$$

where:
$P_{CONTROL(IC)}$ = control IC power dissipation;
I_{CC1} = IC quiescent supply current;
V_{CC1} = IC supply voltage;
$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;
$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses.

The upper (switching) MOSFET gate driver (IC) losses are:

$$P_{GATE(H)} = Q_{GATE(H)} \times f_{SW} \times V_{CC}$$

where:
$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;
$Q_{GATE(H)}$ = total upper MOSFET gate charge at V_{CC};
f_{SW} = switching frequency;

The lower (synchronous) MOSFET gate driver (IC) losses are:

$$P_{GATE(L)} = Q_{GATE(L)} \times f_{SW} \times V_{GATE(L)}$$

where:

$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses;

$Q_{GATE(L)}$ = total lower MOSFET gate charge at V_{CC};

f_{SW} = switching frequency;

The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

Adding External Slope Compensation

Today's voltage regulators are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that very little voltage ramp exists at the control IC feedback pin (V_{FB}), resulting in increased regulator sensitivity to noise and the potential for loop instability. In applications where the internal slope compensation is insufficient, the performance of the CS5421−based regulator can be improved through the addition of a fixed amount of external slope compensation at the output of the PWM Error Amplifier (the COMP pin) during the regulator off−time. Referring to Figure 7, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1and R2.

$$V_{SLOPECOMP} = V_{GATE(L)} \times \left(\frac{R2}{R1 + R2}\right) \times (1.0 - e^{\frac{-t}{\tau}})$$

where:

$V_{SLOPECOMP}$ = amount of slope added;

$V_{GATE(L)}$ = lower MOSFET gate voltage;

R1, R2 = voltage divider resistors;

$t = t_{ON}$ or t_{OFF} (switch off−time);

τ = RC constant determined by C1 and the parallel combination of R1, R2 neglecting the low driver output impedance.

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off−time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of R1 and R2 is high enough in resistance to avoid loading the GATE(L) pin.

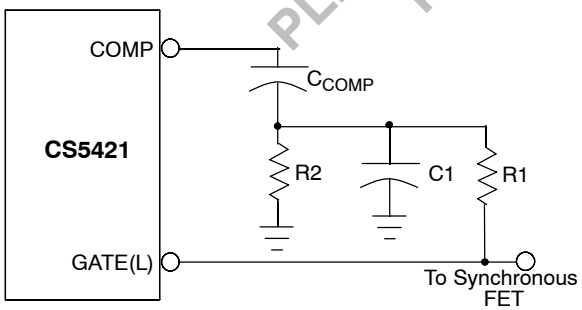


Figure 8. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On−Time Cycle

THERMAL MANAGEMENT

Thermal Considerations for Power MOSFET

As the plastic packaging of a semiconductor will deteriorate at high temperatures, it is necessary to limit the junction temperature of the control IC and power MOSFETs to maintain high reliability. Most semiconductor devices have a maximum junction temperature of 150°C, and manufacturers recommend operating their products at lower temperatures if at all possible.

Power dissipation in a semiconductor devices results in the generation of heat in the pin junctions at the surface of the chip. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the resistive properties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturer's data sheets as Θ_{JA}, or junction−to−air thermal resistance. The on−chip junction temperature can be calculated if Θ_{JA}, the air temperature at the surface of the IC, and the on−chip power dissipation are known.

$$T_J = T_A + (P_D \Theta_{JA})$$

where:

TJ = IC or FET junction temperature (in degrees C);

TA = ambient temperature (in degrees C);

PD = power dissipated by part in question (in watts);

Θ_{JA} = junction−to−ambient thermal resistance (in degrees C per watt).

The value for Θ_{JA} can be found in the Absolute Maximum Ratings table on page 2 of this datasheet. Note that this value is different for every package style and every manufacturer.

The junction temperature should be calculated for all semiconductor devices as a part of the design phase in order to ensure that the devices are operated below the manufacturer's maximum junction temperature specification. If any component's temperature exceeds the manufacturer's maximum temperature, some form of heatsink will be required.

Heatsinking improves the thermal performance of any component. Adding a heatsink will reduce the magnitude of Θ_{JA} by providing a larger surface area for the transfer of heat from the component to the surrounding air. Typical heatsinking techniques include the use of commercial heatsinks for devices in TO−220 packages, or printed circuit board techniques such as thermal bias and large copper foil areas for surface mount packages.

When choosing a heatsink, it is important to realize that Θ_{JA} is comprised of several components:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$$

where:

Θ_{JC} = the junction−to−case thermal resistance (in degrees C per watt);

Θ_{CS} = the case−to−sink thermal resistance (in degrees C per watt);

Θ_{SA} = the sink−to−ambient thermal resistance (in degrees C per watt).

The value for Θ_{JC} is included in the component manufacturer's data sheets. Its value is dependent on the mold compound and lead frames used in assembly of the semiconductor device in question.

Θ_{CS} is the thermal impedance from the surface of the case to the heatsink. This component of the thermal resistance is dependent on the roughness of the heatsink and component as well as on the pressure applied between the two. Θ_{CS} can be reduced by using thermal pads or by applying a thin layer of thermal grease between the case and the heatsink. Such materials reduce the air gap normally found between the heatsink and the case and provide a better path for thermal energy. Values of Θ_{CS} are found in catalogs published by manufacturers of heatsinks and thermal compounds.

Finally, Θ_{SA} is the thermal impedance from the heatsink to the ambient environment. Θ_{SA} is the important parameter when selecting a heatsink. Low values of Θ_{SA} allow increased power dissipation without exceeding the maximum junction temperature of the component. Values of Θ_{SA} are found in catalogs published by heatsink manufacturers.

The basic equation for selecting a heatsink is:

$$P = \frac{T_J - T_A}{\Theta_{JC} + \Theta_{CS} + \Theta_{SA}}$$

where:

P_D = power dissipated by part in question (in watts);

T_J = IC or FET junction temperature (in degrees C);

T_A = ambient temperature (in degrees C);

Θ_{JC} = the junction−to−case thermal resistance (in degrees C per watt);

Θ_{CS} = the case−to−sink thermal resistance (in degrees C per watt);

Θ_{SA} = the sink−to−ambient thermal resistance (in degrees C per watt).

The choice of heatsink is dependent on the value of Θ_{SA} required to keep the calculated junction temperature at the given level of power dissipation below the component manufacturer's maximum junction temperature.

EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

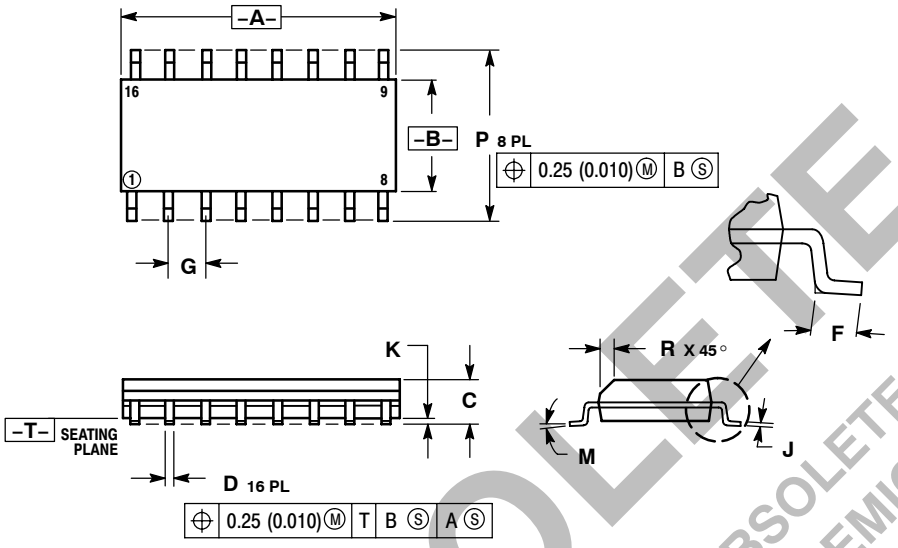
LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS5421.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double−sided PCB's a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCB's are usually sufficient for a good layout, four−layer PCB's are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layers for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the COMP capacitor as close as possible to the COMP pin.
12. Connect the filter components of the following pins: V_{FB}, V_{OUT}, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
13. Place the V_{CC} bypass capacitors as close as possible to the IC.

PACKAGE DIMENSIONS

SO−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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